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Title: Preliminary K20 Test Results

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Preliminary K20 Test Results

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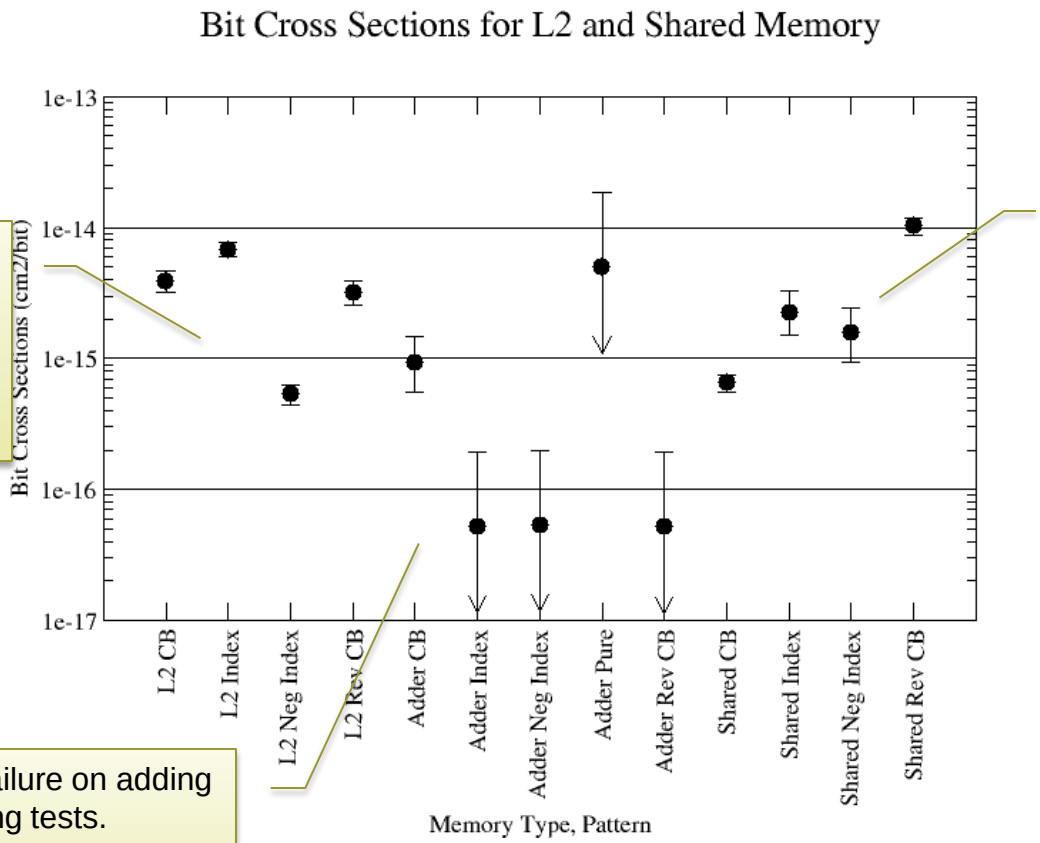
K20 Tests

- **The NVIDIA K20 was tested at the LANSCE ICE House in Sept 2014**
- **The tests focused on characterizing the different types of memories to get an understanding of the underlying neutron sensitivities of the component**

Bit Cross Sections

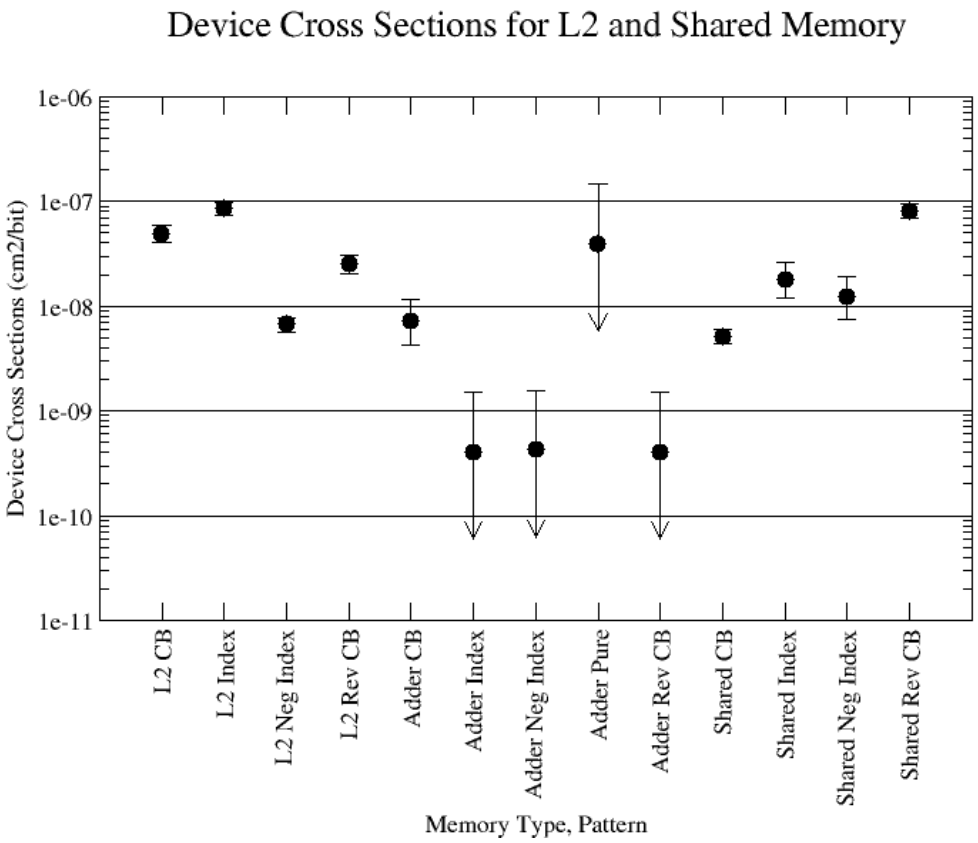


L2 memory sensitivities are lower than expected for some patterns. Indication that there is a preference for 0->1 transitions.

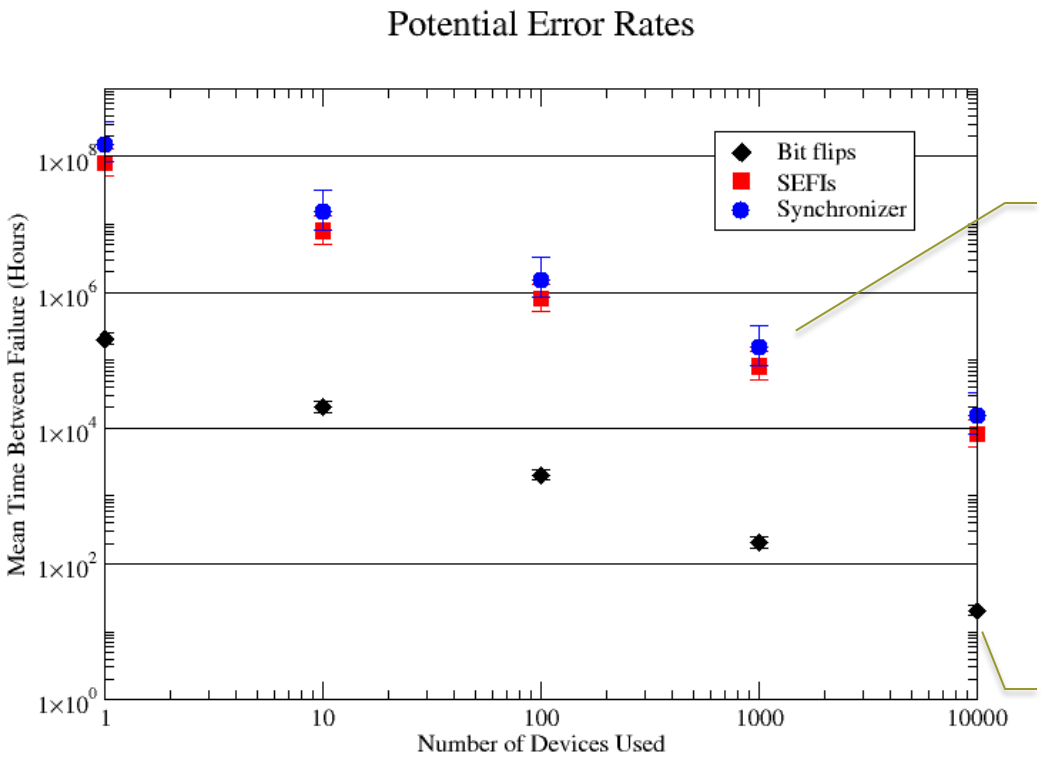
Shared memory sensitivies are different from the L2 memory. Indication that less of a difference between 0->1 transitions and 1->0 transitions.

Only one failure on adding for all adding tests. Failure could have been from a transient or a bitflip in the register space.

Device Cross Sections: Bit Cross Sections Translated to Full Devices



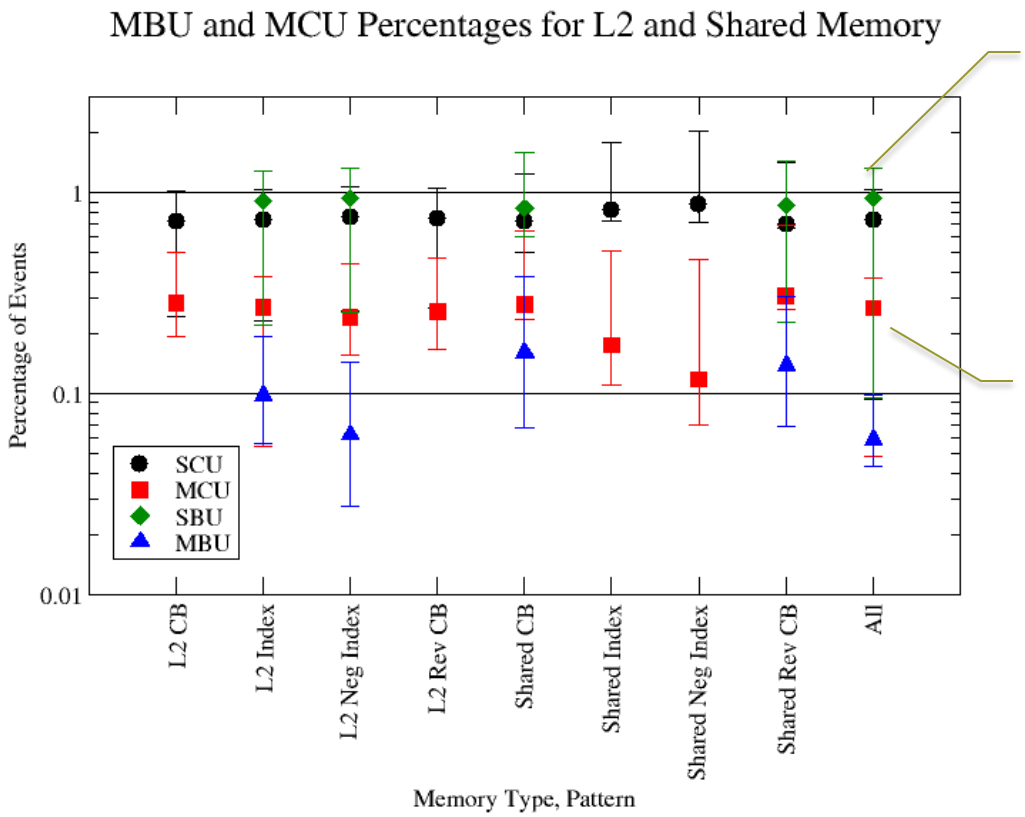
Projected Error Rates



Thread synchronization failures due to radiation are possible, as well as crashing (SEFIs). Both have much lower error rates than just raw bitflips.

Possibly bitflips are only observable in very large clusters. Despite the large amount of memory on these components, the low neutron sensitivity is helping.

Categorization of Single-Event Upsets by Size



Most of the events are "single" type of events – either only one bit or one bit in one word are affected.

No real pattern dependence in MCUs. Most MCUs are not MBUs, which means that ECC should work in many cases.

Affected Bits and Words in Single-Event Upsets

Most MCUs affect 1-4 words. Indication of by-4 interleaving?

Most MBUs affect a widely varying number of bits. Likely suspect are the 1->0 transitions.